What is claimed is:

1. A method of making a semiconductor chip assembly comprising the steps of:

(a) providing a subassembly including a semiconductor chip having a front surface and having contacts on the front surface, and a package element attached to the chip so that a peripheral region of the package element projects outwardly away from the chip in horizontal directions generally parallel to the front face of the chip;

(b) providing a dielectric element having top and bottom surfaces and terminals on the top surface, and positioning the dielectric element to overlie the subassembly with the top surface and terminals facing away from the chip and package element, with a central region of the dielectric element disposed adjacent the chip and with a peripheral region of the dielectric element carrying at least some of the terminals overlying the peripheral region of the package element;

(c) providing first leads attached to the chip at one end thereof and to the dielectric element at the other end thereof, the first leads being electrically connected between the contacts of the chip and the terminals on the dielectric element; and

(d) moving the dielectric element and chip relative to one another through a predetermined displacement so that the dielectric element moves with a vertical component of motion away from the chip, and so that the first leads are bent to a configuration in which each said first lead is flexible ; and

(e) injecting a curable liquid beneath the dielectric element and curing the liquid to form a compliant layer supporting the dielectric element above the chip and package element.

2. A semiconductor chip assembly comprising:

(a) a subassembly including a semiconductor chip having a front surface with contacts thereon and a package element having a central region attached to the chip and a peripheral region extending outwardly away from the chip in horizontal directions generally parallel to the front face of the chip;

(b) a substantially imperforate dielectric element overlying the subassembly, the sheet including a central region overlying the central region of the package element adjacent the chip, and a peripheral region extending outwardly from the central region of the sheet and overlying the peripheral region of the package element, the sheet having a top surface facing away from the subassembly and a bottom surface facing toward the subassembly and electrically conductive terminals on the top surface, at least some of the terminals being disposed in said peripheral region of the sheet;

(c) a compliant layer disposed between the subassembly and dielectric element and supporting the dielectric element above the subassembly; and

(d) vertically-extensive flexible first leads embedded in said compliant layer and extending upwardly from the contacts on the chip to the central region of the dielectric element, the flexible leads being electrically connected to the terminals.